Specifications

Typical for 25 °C unless otherwise specified.

Specifications in *italic text* are guaranteed by design.

Analog input

Table 1. Analog input specifications

A/D converter type	Successive approximation	
Resolution	16 bits	
Number of channels	64 single-ended/32 differential, software-selectable	
Input ranges (SW programmable)	Bipolar: ±10 V, ±5 V, ±2 V, ±1 V , ±0.5 V, ±0.2 V, ±0.1 V	
Maximum sample rate	1 MHz	
Nonlinearity (integral)	±2 LSB maximum	
Nonlinearity (differential)	±1 LSB maximum	
A/D pacing	Onboard input scan clock, external source (XAPCR)	
Trigger sources and modes	See Table 8	
Acquisition data buffer	1 MSample	
Configuration memory	Programmable I/O	
Maximum usable input voltage + common mode voltage (CMV + V_{in})	Range: ±10 V, ±5 V, ±2 V, ±1 V , ±0.5 V	10.5 V maximum
	Range: ±0.2 V, ±0.1 V	2.1 V maximum
Signal to noise and distortion	*72 dB typical for ±10 V range, 1 kHz fundamental*	
Total harmonic distortion	*-80 dB typical for ±10 V range, 1 kHz fundamental*	
Calibration	Auto-calibration, calibration factors for each range stored onboard in non-volatile RAM.	
CMRR @ 60 Hz	-70 dB typical DC to 1 kHz	
Bias current	*40 pA typical (0 °C to 35°C)*	
Crosstalk	*-75 dB typical DC to 60Hz; -65 dB typical @ 10kHz*	
Input impedance	*10 MΩ single-ended, 20 MΩ differential*	
Absolute maximum input voltage	*±30 V*	

Accuracy

Table 2. Analog input accuracy specifications

Voltage range		**Accuracy ±(% of reading + % range) 23°C ±10 °C, 1 year**	**Temperature coefficient ±(ppm of reading + ppm range)/°C**	**Noise (cts RMS)**	
-10 V to 10 V	Note 1	*0.031% + 0.008%*	*14 + 8*	2.0	Note 2
-5 V to 5 V		*0.031% + 0.009%*	*14 + 9*	3.0	
-2 V to 2 V		*0.031% + 0.010%*	*14 +10*	2.0	
-1 V to 1 V		*0.031% + 0.02%*	*14 + 12*	3.5	
-500 mV to 500 mV		*0.031% + 0.04%*	*14 +18*	5.5	
-200 mV to 200 mV		*0.036% + 0.075%*	*14 +12*	8.0	
-100 mV to 100 mV		*0.042% + 0.15%*	*14 +18*	14.0	

Note 1: Specifications assume differential input single-channel scan, 1 MHz scan rate, unfiltered, CMV=0.0 V, 30 minute warm-up, exclusive of noise, range is +FS to -FS.

Note 2: Noise reflects 10,000 samples at 1 MHz, typical, differential short.

Thermocouples

Table 3. TC types and accuracy (Note 3)

TC type	Temperature range (°C)	Accuracy (±°C)	Noise typical (±°C)
J	-200 to + 760	1.7	0.2
K	-200 to + 1200	1.8	0.2
T	-200 to + 400	1.8	0.2
E	-270 to + 650	1.7	0.2
R	-50 to + 1768	4.8	1.5
S	-50 to + 1768	4.7	1.5
N	-270 to + 1300	2.7	0.3
B	+300 to + 1400	3.0	1.0

Note 3: Assumes 16384 oversampling applied, CMV = 0.0V, 60 minute warm-up, still environment, and 25 °C ambient temperature; excludes thermocouple error; TC_{in} = 0 °C for all types except B (1000 °C), PS-9V1AEPS-2500 power supply for external power.

Analog outputs

Analog output channels can be updated synchronously relative to scanned inputs, and clocked from either an internal onboard clock, or an external clock source. Analog outputs can also be updated asynchronously, independent of any other scanning system.

Table 4. Analog output specifications

Channels	4
Resolution	16-bits
Data buffer	PC-based memory
Output voltage range	±10 V
Output current	±1 mA; sourcing more current (1 to 10 mA) may require a PS-9V1AEPS-2500 power supply option
Offset error	±0.0045 V maximum
Digital feed-through	<10 mV when updated
DAC analog glitch	<12 mV typical at major carry
Gain error	±0.01%
Coupling	DC
Update rate	1 MHz maximum, resolution 20.83 ns
Settling time	2 µs to rated accuracy
Pacer sources	Four programmable sources: ▪ Onboard output scan clock, independent of scanning input clock ▪ Onboard input scan clock ▪ External output scan clock (XDPCR), independent of external input scan clock (XAPCR) ▪ External input scan clock (XAPCR)
Trigger sources	Start of input scan

Digital input/output

Table 5. Digital input/output specifications

Number of I/O	24
Ports	Three banks of eight. Each port is programmable as input or output
Input scanning modes	Two programmable ▪ Asynchronous, under program control at any time relative to input scanning ▪ Synchronous with input scanning
Input characteristics	220 Ω series resistors, 20 pF to common
Logic keeper circuit	Holds the logic value to 0 or 1 when there is no external driver
Input protection	±15 kV ESD clamp diodes parallel
Input high	*+2.0 V to +5.0 V*
Input low	*0 to 0.8 V*
Output high	*>2.0 V*
Output low	*<0.8 V*
Output current	Output 1.0 mA per pin, sourcing more current may require a PS-9V1AEPS-2500 power supply option
Digital input pacing	Onboard clock, external input scan clock (XAPCR)
Digital output pacing	Four programmable sources: ▪ Onboard output scan clock, independent of input scan clock ▪ Onboard input scan clock ▪ External output scan clock (XDPCR), independent of external input scan clock (XAPCR) ▪ External input scan clock (XAPCR)
Digital input trigger sources and modes	See Table 8
Digital output trigger sources	Start of input scan
Sampling/update rate	4 MHz maximum (rates up to 12 MHz are sustainable on some platforms)
Pattern generation output	Two of the 8-bit ports can be configured for 16-bit pattern generation. The pattern can also be updated synchronously with an acquisition at up to 4 MHz.

Counters

Counter inputs can be scanned based on an internal programmable timer or an external clock source.

Table 6. Counter specifications

Channels	Four independent
Resolution	32-bit
Input frequency	20 MHz maximum
Input signal range	-5 V to 10 V
Input characteristics	10 kΩ pull-up, ±15 kV ESD protection
Trigger level	TTL
Minimum pulse width	25 ns high, 25 ns low
De-bounce times	16 selections from 500 ns to 25.5 ms, positive or negative edge sensitive, glitch detect mode or de-bounce mode
Time-base accuracy	50 ppm (0 ° to 50 °C)
Counter read pacer	Onboard input scan clock, external input scan clock (XAPCR)
Trigger sources and modes	See Table 8
Programmable mode	Counter
Counter mode options	Totalize, clear on read, rollover, stop at all Fs, 16-bit or 32-bit, any other channel can gate the counter

Input sequencer

Analog, digital, and counter inputs can be scanned based on either an internal programmable timer or an external clock source.

Table 7. Input sequencer specifications

Input scan clock sources: two (see Note 4)	Internal: ▪ Analog channels from 1 µs to 1 sec in 20.83 ns steps. ▪ Digital channels and counters from 250 ns to 1 sec in 20.83 ns steps. External. TTL level input (XAPCR): ▪ Analog channels down to 1 µs minimum ▪ Digital channels and counters down to 250 ns minimum
Programmable parameters per scan:	Programmable channels (random order), programmable gain
Depth	512 locations
Onboard channel to channel scan rate	Analog: 1 MHz maximum Digital: 4 MHz if no analog channels are enabled, 1 MHz with analog channels enabled
External input scan clock (XAPCR) maximum rate	Analog: 1MHz Digital: 4 MHz if no analog channels are enabled, 1 MHz with analog channels enabled
Clock signal range:	Logical zero: 0 V to 0.8 V Logical one: 2.4 V to 5.0 V
Minimum pulse width	50 ns high, 50 ns low

Note 4: The maximum scan clock rate is the inverse of the minimum scan period. The minimum scan period is equal to 1 µs times the number of analog channels. If a scan contains only digital channels, then the minimum scan period is 250 ns.

Some platforms can sustain scan rates up to 83.33 ns for digital-only scans.

Trigger sources and modes

Table 8. Trigger sources and modes

Input scan trigger sources	▪ Single channel analog hardware trigger ▪ Single channel analog software trigger ▪ External-single channel digital trigger (TTL TRG input) ▪ Digital Pattern Trigger ▪ Counter/Totalizer Trigger
Input scan triggering modes	▪ Single channel analog hardware trigger: The first analog input channel in the scan is the analog trigger channel Input signal range: -10 V to +10 V maximum Trigger level: Programmable (12-bit resolution) Latency: 350 ns typical Accuracy: ±0.5% of reading, ±2 mV offset maximum Noise: 2 mV RMS typical
	▪ Single channel analog software trigger: The first analog input channel in the scan is the analog trigger channel Input signal range: Anywhere within range of the trigger channel Trigger level: Programmable (16-bit resolution) Latency: One scan period (maximum)
	▪ External-single channel digital trigger (TTL trigger input): Input signal range: -15 V to +15 V maximum Trigger level: TTL level sensitive Minimum pulse width: 50 ns high, 50 ns low Latency: One scan period maximum
	▪ Digital Pattern Triggering 8-bit or 16-bit pattern triggering on any of the digital ports. Programmable for trigger on equal, not equal, above, or below a value. Individual bits can be masked for "don't care" condition. Latency: One scan period, maximum
	▪ Counter/Totalizer Triggering Counter/totalizer inputs can trigger an acquisition. User can select to trigger on a frequency or on total counts that are equal, not equal, above, or below a value, or within/outside of a window rising/falling edge. Latency: One scan period, maximum

Frequency/pulse generators

Table 9. Frequency/pulse generator specifications

Channels	2 x 16-bit
Output waveform	Square wave
Output rate	1 MHz base rate divided by 1 to 65535 (programmable)
High-level output voltage	2.0 V minimum @ -1.0 mA, 2.9 V minimum @ -400 µA
Low-level output voltage	0.4 V maximum @ 400 µA

Power consumption

Table 10. Power consumption specifications (Note 5)

Power consumption (per board)	3400 mW

External power

Table 11. External power specifications (Note 5)

Connector	Switchcraft # RAPC-712
Power range	6 to 16 VDC (used when USB port supplies insufficient power, or when an independent power supply is desired)
Over-voltage	20 V for 10 seconds, maximum

Note 5: An optional power supply (MCC p/n PS-9V1AEPS-2500) is required if the USB port cannot supply adequate power. USB 2.0 ports are, by USB 2.0 standards, required to supply 2500 mW (nominal at 5 V, 500 mA)

USB specifications

Table 12. USB specifications

USB-device type	USB 2.0 high-speed mode (480 Mbps) if available (recommended), otherwise, USB 1.1 full-speed mode (12 Mbps)
Device compatibility	USB 2.0 (recommended) or USB 1.1

Environmental

Table 13. Environmental specifications

Operating temperature range	-30 °C to +70 °C
Storage temperature range	-40 °C to +80 °C
Relative humidity	0 to 95% non-condensing

Mechanical

Table 14. Mechanical specifications

Vibration	MIL STD 810E cat 1 and 10
Dimensions	152.4 mm (W) x 150.62 mm (D) (6.0” x 5.93”)
Weight	147 g (0.32 lbs)

Signal I/O connectors and pin out

Table 15. Main connector specifications

Connector type	68-pin standard "SCSI TYPE III" female connector (P5); four 40-pin headers (J5, J6, J7, J8), AMP# 2-103328-0
Temperature measurement connector	4-channel TC screw-terminal block (TB7); Phoenix # MPT 0.5/9-2.54
Compatible cables (for the 68-pin SCSI connector)	CA-68-3R — 68-pin ribbon cable; 3 feet. CA-68-3S — 68-pin shielded round cable; 3 feet. CA-68-6S — 68-pin shielded round cable; 6 feet.
Compatible cables (for the 40-pin header connectors)	C40FF-#
Compatible accessory products (for the 68-pin SCSI connector)	TB-100 termination board with screw terminals
	RM-TB-100, 19-inch rack mount kit for TB-100
Compatible accessory products (for the 40-pin header connectors)	CIO-MINI40

68-pin SCSI connector pin outs

Table 16. 68-pin SCSI connector pin out (labeled P5 on the board)
single-ended mode

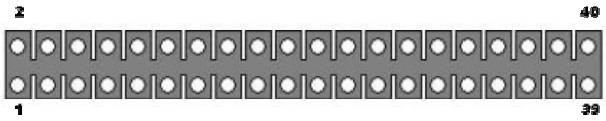
Pin	Function	Pin	Function
68	ACH0	34	ACH8
67	AGND	33	ACH1
66	ACH9	32	AGND
65	ACH2	31	ACH10
64	AGND	30	ACH3
63	ACH11	29	AGND
62	SGND (low level sense - not for general use)	28	ACH4
61	ACH12	27	AGND
60	ACH5	26	ACH13
59	AGND	25	ACH6
58	ACH14	24	AGND
57	ACH7	23	ACH15
56	XDAC3	22	XDAC0
55	XDAC2	21	XDAC1
54	NEGREF (reserved for self-calibration)	20	POSREF (reserved for self-calibration)
53	GND	19	+5 V (see Note 6)
52	A1	18	A0
51	A3	17	A2
50	A5	16	A4
49	A7	15	A6
48	B1	14	B0
47	B3	13	B2
46	B5	12	B4
45	B7	11	B6
44	C1	10	C0
43	C3	9	C2
42	C5	8	C4
41	C7	7	C6
40	GND	6	TTL TRG
39	CNT1	5	CNT0
38	CNT3	4	CNT2
37	TMR1	3	TMR0
36	GND	2	XAPCR (input scan clock)
35	GND	1	XDPCR (output scan clock)

Table 17. 68-pin SCSI connector pin out (labeled P5 on the board)
differential mode

Pin	Function	Pin	Function
68	ACH0 HI	34	ACH0 LO
67	AGND	33	ACH1 HI
66	ACH1 LO	32	AGND
65	ACH2 HI	31	ACH2 LO
64	AGND	30	ACH3 HI
63	ACH3 LO	29	AGND
62	SGND (not for general use)	28	ACH4 HI
61	ACH4 LO	27	AGND
60	ACH5 HI	26	ACH5 LO
59	AGND	25	ACH6 HI
58	ACH6 LO	24	AGND
57	ACH7 HI	23	ACH7 LO
56	XDAC3	22	XDAC0
55	XDAC2	21	XDAC1
54	NEGREF (reserved for self-calibration)	20	POSREF (reserved for self-calibration)
53	GND	19	+5 V (see Note 6)
52	A1	18	A0
51	A3	17	A2
50	A5	16	A4
49	A7	15	A6
48	B1	14	B0
47	B3	13	B2
46	B5	12	B4
45	B7	11	B6
44	C1	10	C0
43	C3	9	C2
42	C5	8	C4
41	C7	7	C6
40	GND	6	TTL TRG
39	CNT1	5	CNT0
38	CNT3	4	CNT2
37	TMR1	3	TMR0
36	GND	2	XAPCR (input scan clock)
35	GND	1	XDPCR (output scan clock)

Note 6: 5 V output, ±20% tolerance, 2mA USB powered, 10mA using external power.

40-pin header connector pin outs



This edge of the header is closest to the center of the USB-2537. Pins 2 and 40 are labeled on the board silkscreen.

J5

Table 18. 40-pin header connector pinout (labeled J5 on the board)
64-channel single-ended mode

Pin	Function	Pin	Function
1	ACH27	2	ACH19
3	ACH26	4	ACH18
5	AGND	6	AGND
7	ACH3	8	ACH11
9	ACH2	10	ACH10
11	ACH17	12	ACH25
13	ACH16	14	ACH24
15	ACH1	16	ACH9
17	ACH0	18	ACH8
19	AGND	20	AGND
21	ACH23	22	ACH31
23	ACH22	24	ACH30
25	ACH7	26	ACH15
27	ACH6	28	ACH14
29	AGND	30	ACH21
31	ACH29	32	ACH20
33	ACH28	34	ACH5
35	ACH13	36	ACH4
37	ACH12	38	AGND
39	AGND	40	AGND

Table 19. 40-pin header connector pinout (labeled J5 on the board)
32-channel differential mode

Pin	Function	Pin	Function
1	ACH11 LO	2	ACH11 HI
3	ACH10 LO	4	ACH10 HI
5	AGND	6	AGND
7	ACH3 HI	8	ACH3 LO
9	ACH2 HI	10	ACH2 LO
11	ACH9 HI	12	ACH9 LO
13	ACH8 HI	14	ACH8 LO
15	ACH1 HI	16	ACH1 LO
17	ACH0 HI	18	ACH0 LO
19	AGND	20	AGND
21	ACH15 HI	22	ACH15 LO
23	ACH14 HI	24	ACH14 LO
25	ACH7 HI	26	ACH7 LO
27	ACH6 HI	28	ACH6 LO
29	AGND	30	ACH13 HI
31	ACH13 LO	32	ACH12 HI
33	ACH12 LO	34	ACH5 HI
35	ACH5 LO	36	ACH4 HI
37	ACH4 LO	38	AGND
39	AGND	40	AGND

J6

Table 20. 40-pin header connector pinout (labeled J6 on the board)
64-channel single-ended mode

Pin	Function	Pin	Function
1	ACH43	2	ACH59
3	ACH35	4	ACH51
5	AGND	6	ACH58
7	ACH42	8	ACH50
9	ACH34	10	ACH57
11	AGND	12	ACH49
13	ACH41	14	ACH56
15	ACH33	16	ACH48
17	ACH40	18	AGND
19	ACH32	20	ACH63
21	ACH47	22	ACH55
23	ACH39	24	AGND
25	ACH46	26	ACH62
27	ACH38	28	ACH54
29	AGND	30	ACH61
31	ACH45	32	ACH53
33	ACH37	34	ACH60
35	ACH44	36	ACH52
37	ACH36	38	AGND
39	AGND	40	AGND

Table 21. 40-pin header connector pinout (labeled J6 on the board)
32-channel differential mode

Pin	Function	Pin	Function
1	ACH19 LO	2	ACH27 LO
3	ACH19 HI	4	ACH27 HI
5	AGND	6	ACH26 LO
7	ACH18 LO	8	ACH26 HI
9	ACH18 HI	10	ACH25 LO
11	AGND	12	ACH25 HI
13	ACH17 LO	14	ACH24 LO
15	ACH17 HI	16	ACH24 HI
17	ACH16 LO	18	AGND
19	ACH16 HI	20	ACH31 LO
21	ACH23 LO	22	ACH31 HI
23	ACH23 HI	24	AGND
25	ACH22 LO	26	ACH30 LO
27	ACH22 HI	28	ACH30 HI
29	AGND	30	ACH29 LO
31	ACH21 LO	32	ACH29 HI
33	ACH21 HI	34	ACH28 LO
35	ACH20 LO	36	ACH28 HI
37	ACH20 HI	38	AGND
39	AGND	40	AGND

J7

Table 22. 40-pin header connector pin out (labeled J7 on the board)

Pin	Function	Pin	Function
1	GND	2	XAPCR (input scan clock)
3	A0	4	A4
5	A1	6	A5
7	A2	8	A6
9	A3	10	A7
11	GND	12	TTL TRG
13	B0	14	B4
15	B1	16	B5
17	B2	18	B6
19	B3	20	B7
21	GND	22	+5 V (see Note 7)
23	C0	24	C4
25	C1	26	C5
27	C2	28	C6
29	C3	30	C7
31	GND	32	TMR1
33	TMR0	34	CNT1
35	CNT0	36	CNT3
37	CNT2	38	GND
39	GND	40	GND

J8

Table 23. 40-pin header connector pin out (labeled J8 on the board)

Pin	Function	Pin	Function
1	+13 V (see Note 8)	2	-13 V (see Note 8)
3	NC	4	NC
5	AGND	6	AGND
7	XDAC0	8	XDAC2
9	XDAC1	10	XDAC3
11	AGND	12	AGND
13	SelfCal	14	SGND (low level sense - not for general use)
15	AGND	16	AGND
17	TTL TRG	18	XDPCR (output scan clock)
19	XAPCR (input scan clock)	20	GND (digital)
21	GND (digital)	22	GND (digital)
23	NC	24	NC
25	+5 V (see Note 7)	26	AUX PWR (output - reserved)
27	NC	28	NC
29	NC	30	NC
31	NC	32	NC
33	NC	34	NC
35	NC	36	NC
37	NC	38	NC
39	NC	40	NC

Note 7: 5 V output, ±20% tolerance, 2mA USB powered, 10mA using external power.

Note 8: ±13 V outputs, ±10% tolerance, 1 mA USB powered, 5 mA using external power

TC connector pin out (TB7)

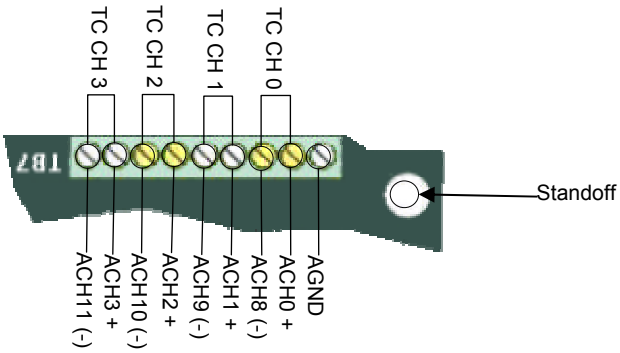


Figure 1. TC terminal pin out (labeled TB7)