Electrical Specifications USB-1604HS

Typical for 25 °C unless otherwise specified.

Analog input

Table 1. Analog input specifications

Parameter	Conditions	Specification
A/D converter type		16-bit successive approximation type
Number of AI channels		4 SE simultaneous
Input configuration		Individual A/D per channel
Sampling method		Simultaneous
Input ranges		±10 V, ±2.5 V, ±500 mV
Analog input modes		SE
Absolute maximum input voltage		±30 V maximum (power on) ±20 V maximum (power off)
Input impedance		100 MΩ (power on)
Input bandwidth (-3 dB)		3 MHz
Digital A/D pacing types		Onboard A/D clock or external source. See Table 5
Trigger sources and modes		See Table 4
Sampling rate		0 to 1.33 MS/s each channel, software programmable
Clock modes		Internal, software programmable or ext pacing
Max throughput		5 MS/s typical, 8 MS/s maximum
Resolution		16 bits
Calibrated accuracy		0.01% FSR
INL		±2.0 LSB maximum
DNL		±1.0 LSB maximum
Noise, CTS, rms	Note 1	±10 V range: < ±2 LSB, ±500 mV range: <±6 LSB
SINAD		86/80 dB typical/minimum
ENOB		14/13 bits typical/minimum
SFDR		86/80 dB typical/minimum

Note 1: Noise distribution is determined by gathering 50k samples with inputs tied to ground at the user connector. Samples are gathered at the maximum specified sampling rate of 2 MS/s.

Analog input calibration

Table 2. Analog input calibration specifications

Parameter	Specifications
Recommended warm-up time	15 minutes minimum
Calibration methods	Software system calibration and self-cal
Self-cal interval	User selectable, manual or periodic
Software system calibration interval	1 year
Software system calibration reference	-10V to +10V programmable. Actual measured values stored in EEPROM.
	Tempco: 5 ppm/°C maximum
	Long term stability: 30 ppm/1000 h

Digital input/output, DIO

Table 3. Digital I/O specifications

Number of I/O	32: 16 inputs, 16 outputs
Digital type	3.3 V CMOS (5 V tolerant)
Digital I/O transfer rate (system-paced)	Up to 8 MHz
Input high voltage	2.0 V to 5.0 V
Input low voltage	0 to 0.8 V
Absolute max input voltage	30 V
Output high voltage (IOH = –1 mA)	>2.0 V
Output low voltage (IOL = 1 mA)	< 0.8 V maximum
Output current	2.5 mA maximum per pin
DIO pacing	On-board or external clock
DIO trigger modes and sources	See Table 5
Input pull-up/pull-down configuration	PCB jumper
Outputs at power on and reset	Low

Trigger sources

Table 4. External trigger specifications

Parameter	**Specification**
Available trigger sources	▪ Analog input hardware (via standard analog input) ▪ Analog software trigger ▪ External digital input ▪ Digital pattern ▪ Counter/totalizer
Trigger source details	
Analog input (hardware) trigger	▪ Input signal range: -10 V to +10 V maximum ▪ Trigger level: Programmable (12-bit resolution) ▪ Latency: 350 ns typical ▪ Accuracy: ±0.5% of reading, ±2 mV offset, maximum ▪ Uncertainty: 2 mV RMS typical
Analog software trigger	▪ Trigger range: Anywhere within range of the trigger channel ▪ Trigger level: Programmable (16-bit resolution) ▪ Latency: one sample period, maximum
External-single channel digital	▪ Input signal range: -15 V to +15 V maximum ▪ Trigger level: TTL level sensitive ▪ Minimum pulse width: 50 ns high, 50 ns low ▪ Latency: One sample period, maximum
Digital pattern triggering	▪ 16-bit pattern triggering on the digital port. ▪ Programmable for trigger on equal, not equal, above, or below a value. ▪ Individual bits can be masked for "don’t care" condition. ▪ Latency: One sample period, maximum
Counter/totalizer triggering	▪ Counter/totalizer inputs can trigger an acquisition. User can select to trigger on a frequency or on total counts that are equal, not equal, above, or below a value, or within/outside of a window rising/falling edge. ▪ Latency: One sample period, maximum

External clock input/output

Table 5. External clock I/O specifications

Parameter	Conditions	Specification
Input clock rate		1.33 MHz maximum
Minimum clock pulse width		50 nS high/50 nS low
Input leakage current		±2.0 µA
Input high voltage		2.4 to 5.0 V
Input low voltage		0 to 0.8 V
Clock sync output high voltage	IOH = 1 mA	>2.0 V
Clock sync output low voltage	IOL = 1 mA	<0.8 V

Counters

Table 6. Counter specifications

Parameter	Specification
Number of channels	4 counters, configurable as 2 gated counters
Modes	Counter, Period, Pulse width, Timing
Counter mode options	Totalize, Clear on Read, Rollover, Stop at Top, 16-bit or 32-bit, any other channel can decrement the counter
Period mode options	Measure x1, x10, x100, or x1000 periods, 16-bit or 32-bit, 4 time bases to choose from (20.83 ns, 208.3 ns, 2.083 µs, 20.83 µs), any other channel can gate the period measurement
Pulse width mode options	16-bit or 32-bit values, 4 time bases to choose from (20.83 ns, 208.3 ns, 2.083 µs, 20.83 µs), any other channel can gate the pulse width measurement
Timing mode options	16-bit or 32-bit values, 4 time bases to choose from (20.83 ns, 208.3 ns, 2.083 µs, 20.83 µs)
Resolution	16-bit or 32-bit
Maximum input frequency	20 MHz
Input type	TTL, rising edge triggered
Input range	-5 V to +10 V
Absolute max input voltage	30 V
De-bounce function	16 selections, from 500 ns to 25.5 ms, positive or negative edge, glitch detect and/or de-bounce modes
Required input current	±5 µA
Minimum pulse width	25 nS high, 25 ns low
Input high voltage	2.4 V to +10 V
Input low voltage	0 to 0.8 V

Timers, frequency, pulse, pwm generators

Table 7. Timers, frequency, pulse, pwm generators specifications

Parameter	Conditions	Specification
Number of channels		2
Effective frequency range		.01 Hz to 24 MHz
Pulse width resolution		20.83 nS
PWM duty cycle range		0 to 100% (variable in 20.83 nS increments)
Minimum pulse width		20.83 nS
Maximum pulse width		100%
Output high voltage	IOH = 1 mA	>2.0 V
Output low voltage	IOL = 1 mA	<0.8 V

Quadrature detectors

Table 8. Quadrature detector specifications

Parameter	Conditions	Specification
Number of detectors		3
Signals per detector		A, B and Z (0°, 90° and zero)
Resolution		16-bit or 32-bit
Maximum frequency		20 MHz
Minimum pulse width		25 nS high, 25 ns low
De-bounce function		16 selections, from 500 ns to 25.5 ms, pos or neg edge, glitch detect and/or de-bounce modes
Input high voltage		2.4 V to +10 V
Input low voltage		0 to 0.8 V
Absolute max input voltage		30 V

Power

Table 9. Power specifications

Parameter	Conditions	Specification
Supply current	Continuous mode	1.5 Amp maximum
+5V EXT output voltage range		4.5 V to 5.25 V
External power supply	MCC p/n PS-5V2AEPS (included)	+5 VDC, 10 W, 5% regulation

USB specifications

Table 10. USB specifications

Parameter	Specification
USB device type	USB 2.0 (high-speed)
USB device compatibility	USB 1.1, 2.0
USB cable length	Three meters maximum
USB cable type	A-B cable, UL type AWM 2527 or equivalent (minimum 24 AWG VBUS/GND, minimum 28 AWG D+/D-)

Environmental

Table 11. Environmental specifications

Parameter	Specification
Operating temperature range	0 to 55 °C maximum
Storage temperature range	-40 to 85 °C maximum
Humidity	0 to 90% non-condensing

Mechanical

Table 12. Mechanical specifications

Dimensions	142.24 mm W x 180.34 mm D x 38.1 mm H (5.6" x 7.1" x 1.5")
Weight	675 g (1.5 lbs)

Signal connectors

BNC signal connectors

Table 13. BNC connector specifications

BNC Signals
Analog input CH0
Analog input CH1
Analog input CH2
Analog input CH3
System Trigger
Pacer Clock

68-pin SCSI signal connector

Table 14. 68-pin SCSI connector pin out

Pin No.	Signal	Pin No.	Signal
1	AGND	35	AGND
2	ACH0	36	ACH2
3	AGND	37	AGND
4	ACH1	38	ACH3
5	AGND	39	AGND
6	VCAL	40	NC
7	AGND	41	NC
8	+5VOUT	42	AGND
9	DIN0	43	DOUT0
10	DIN1	44	DOUT1
11	DIN2	45	DOUT2
12	DIN3	46	DOUT3
13	DIN4	47	DOUT4
14	DIN5	48	DOUT5
15	DIN6	49	DOUT6
16	DIN7	50	DOUT7
17	DIN8	51	DOUT8
18	DIN9	52	DOUT9
19	DIN10	53	DOUT10
20	DIN11	54	DOUT11
21	DIN12	55	DOUT12
22	DIN13	56	DOUT13
23	DIN14	57	DOUT14
24	DIN15	58	DOUT15
25	CTR4 A	59	CTR0
26	CTR4 B	60	CTR1
27	CTR4 Z	61	CTR2
28	CTR5 A	62	CTR3
29	CTR5 B	63	TMR/PWM0
30	CTR5 Z	64	TMR/PWM1
31	CTR6 A	65	DIG TRIG
32	CTR6 B	66	XAPCR
33	CTR6 Z	67	XDPCR
34	DGND	68	DGND